Digital IQ demodulator

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Operating with integrated zero-IF signal
- Operating with FSK and GFSK modulated signals
- Built-in clock former
- Low current consumption: 80 uA at a voltage of 1.8 V and input sampling frequency is 40kHz
- Test modes
- Transmission speed is 2400 baud
- High noise immunity
- Wide deviation range: 2.5…7 kHz
- Wide detuning range: up to 1.5 kHz at 4 kHz deviation
- Independent automatic gain control for each channel
- Built-in independent DC component compensation
- Operating in a pulsed mode (hot start)
- Small area: 0.9 mm^2
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

2 APPLICATION

- Receivers with FSK, GFSK modulation
- Digital signal processors
- System on a chip

3 OVERVIEW

The digital IQ demodulator is used to demodulate frequency-modulated signal. The device operates with 2^{nd} order delta-sigma ADC, with following decimation and filtering the digitized signal. The input signal is a dual (I and Q) with zero IF, 16-bit. It is allowed DC component (see subsection 7.2), which is automatically rebuilt by input stages. The output demodulated signal is given to the out from quadrature demodulator.
Using the receiver in a pulse mode is possible when the last values of gain and DC component are stored in registers.
Necessary clock frequencies are generated from input clock signal.
The output signal is an asynchronous bit stream. Typical transmission speed is 2400 baud.
The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

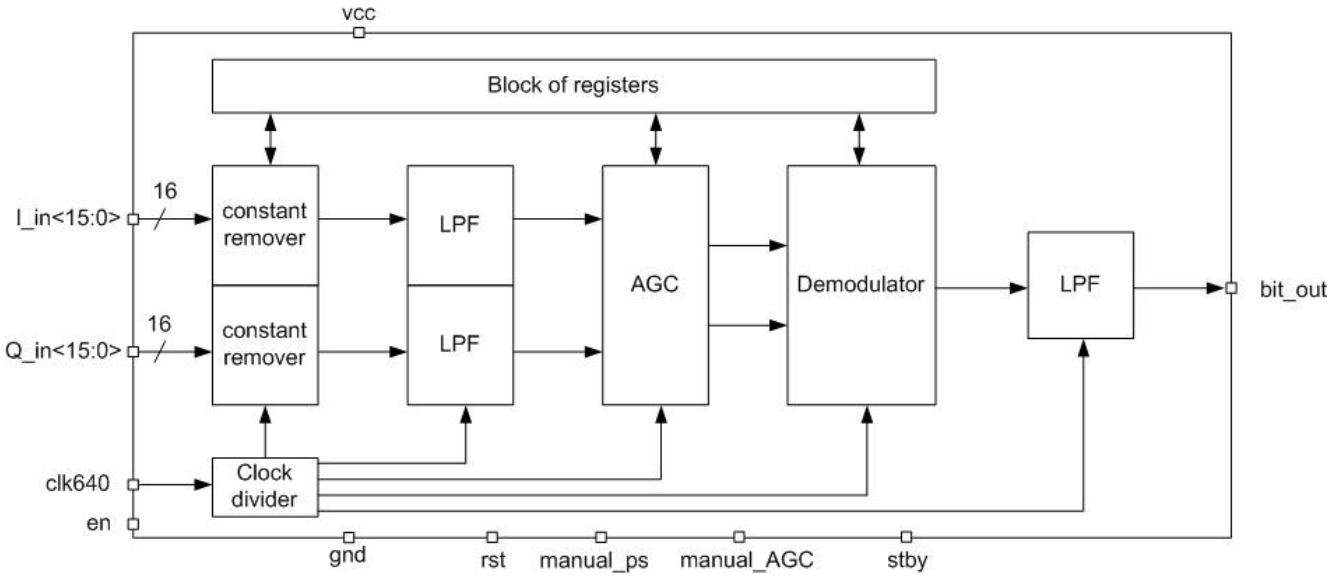

Figure 1: Digital IQ demodulator structure.

5 PIN DESCRIPTION

Name	Direction	Description
clk640	I	External clock input
rst	I	Reset
en	I	Enable/disable
manual_ps	I	Manual mode enable for constant remover
manual_AGC	I	Manual mode enable for AGC
stby	I	Standby mode enable/disable
I_in<15:0>	I	I-channel input
Q_in<15:0>	I	Q-channel input
bit_out	O	Circuit output (bit stream)
vcc	IO	Supply voltage
gnd	IO	Ground

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions.

Dimension	Value	Unit
Height	1816	um
Width	523	um

Figure 2: Digital IQ demodulator layout view.

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ iHP SiGe BiCMOS 0.25 um
Status _____ silicon proven
Area _____ 0.9 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.5 ÷ 2.7 V and T_a = -45 ÷ +85 °C. Typical values are at V_{cc} = 1.8 V, T_a = 27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	1.5	1.8	2.7	V
Operating temperature range	T_a	-	-45	27	85	°C
External synchronizing frequency	F_{CLK}	-	-	640	-	kHz
Input sampling frequency	F_S	-	-	40	-	kHz
Input resolution	N	-	-	16	-	bit/channel
Useful signal to signal interference ratio*	-	BER<7%	-	-25	-	dB
Build-in AGC maximum gain	-	-	-	80	-	dB
Current consumption	I_{cc}	-	-	80	-	uA
Input logic-high level	V_{IH}	-	$0.7V_{cc}$	-	V_{cc}+0.25	V
Input logic-low level	V_{IL}		-0.25	-	0.3	V

* The frequency modulated signal: modulating signal – a sine, frequency 400 Hz, deviation 2400Hz, central frequency 20 kHz.

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optinal)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optinal)
- Documentation