Digital filter with input sampling rate 2.56 MHz

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Built-in clock former
- Test modes – digital data output
- Operating with complex signal
- Low current consumption: 80 uA at the input sampling rate 2.56 MHz
- Small area: 1.4 mm^2 and supply voltage is 1.8 V
- Input data - the delta-sigma modulated signal
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

2 APPLICATION

- Delta-sigma ADC
- Systems using a delta-sigma modulator signal as an input data

3 OVERVIEW

Block consists of 4 serially connected low pass filters. Decimation takes place during a filtration process after each stage. The total decimation coefficient is 64.
The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

Table 1: Stage parameters of digital filters

Parameter	CIC-filter (the first stage)	FIR-filter (the second stage)	FIR-filter (the third stage)	FIR-filter (the forth stage)
Input data	1 bit	16 bit	16 bit	16 bit
Output data	10 bit	16 bit	16 bit	16 bit
Band pass	60 kHz	30 kHz	15 kHz	12 kHz
Amplitude ripple*	0.01 dB	0.02 dB	0.07 dB	0.004 dB
Reject band	>320 kHz	>80 kHz	>40 kHz	>20 kHz
Signal attenuation**	≥40 dB	≥80 dB	≥76 dB	≥95 dB

* In band pass up to 5 kHz
** Depends on reject band
Sampling rate is redoubled at the stages output.

Amplitude-frequency characteristic of stages is shown in figures 1-4.

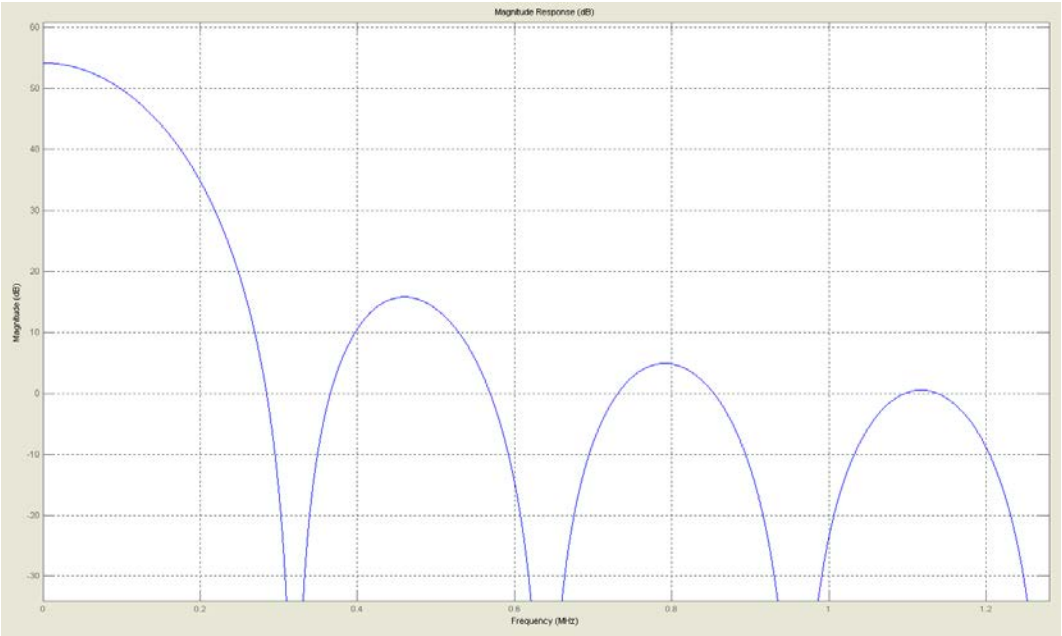

Figure 1: Amplitude-frequency characteristic of the first stage.

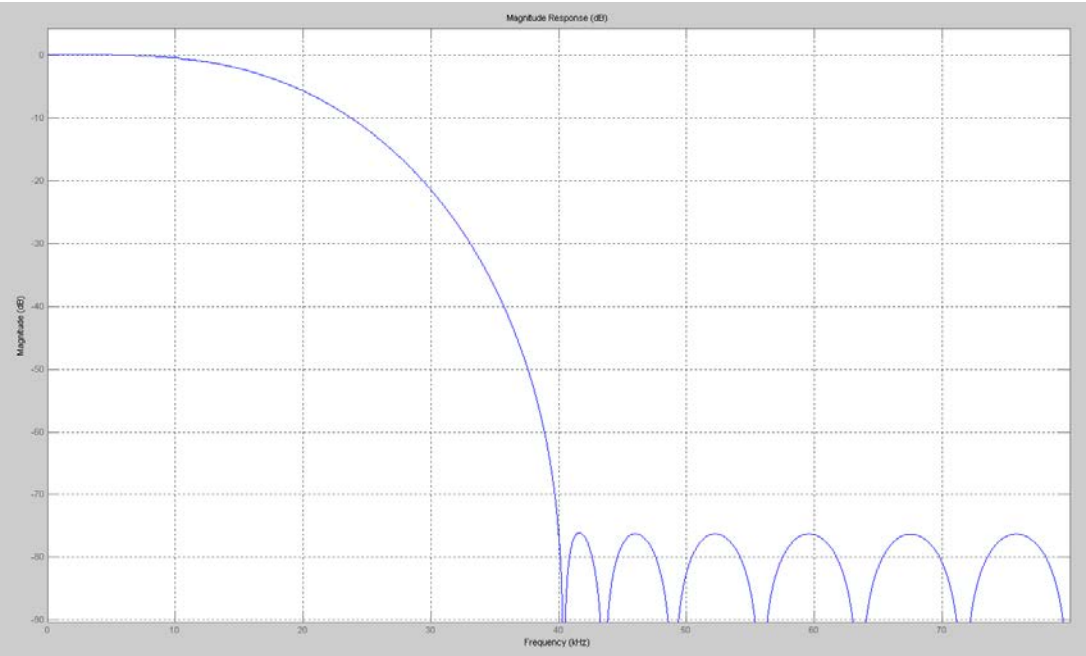

Figure 2: Amplitude-frequency characteristic of the second stage.

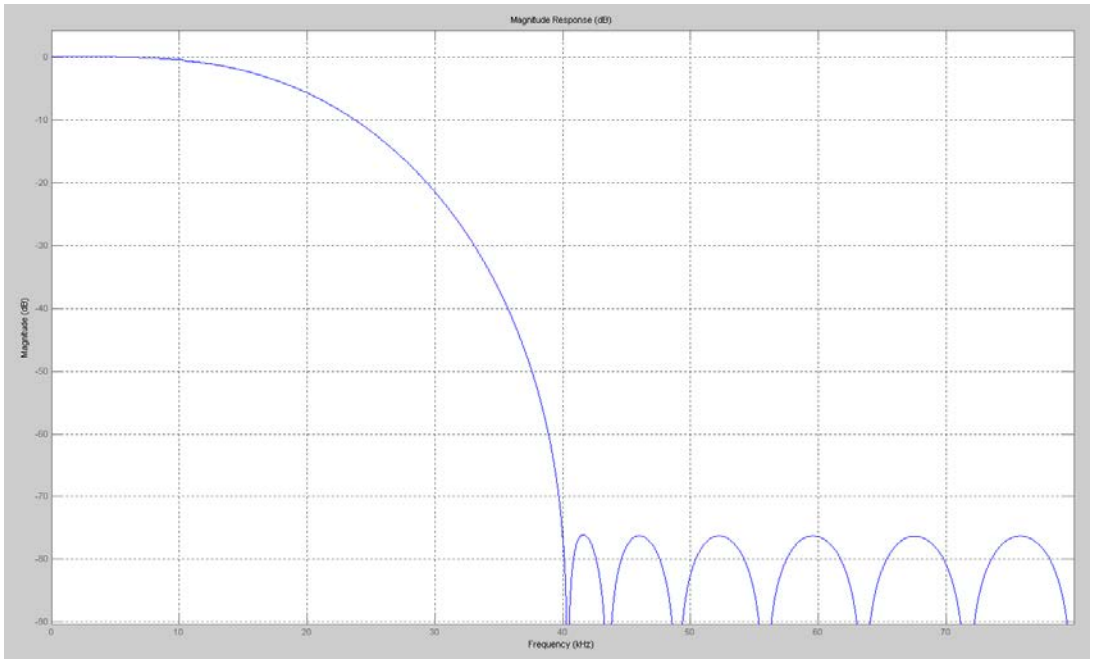

Figure 3: Amplitude-frequency characteristic of the third stage.

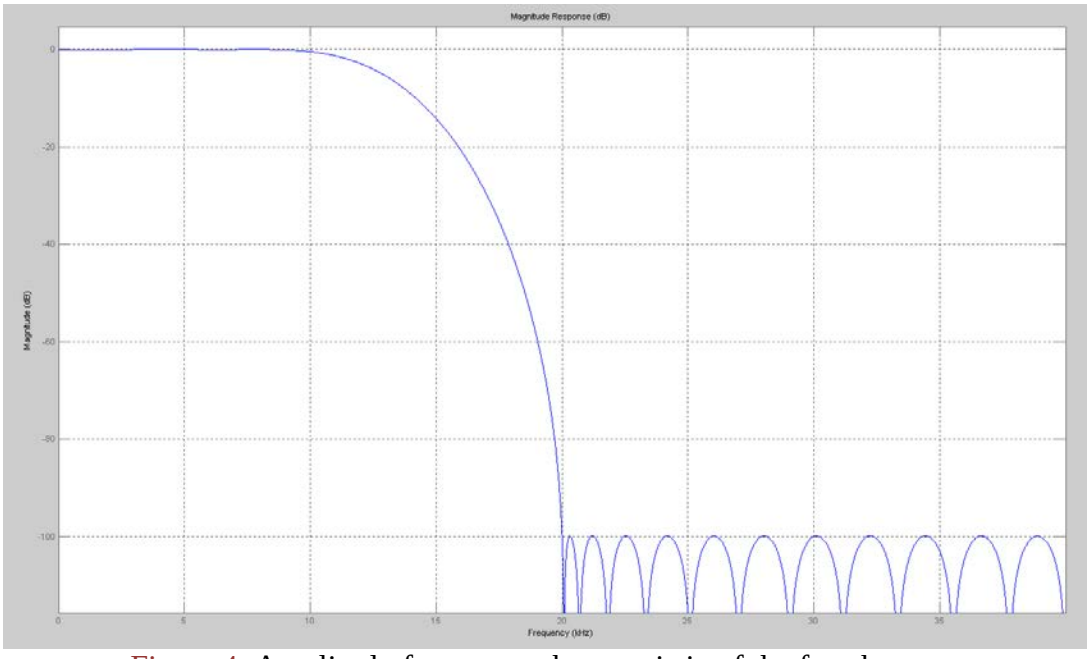

Figure 4: Amplitude-frequency characteristic of the fourth stage.

4 STRUCTURE

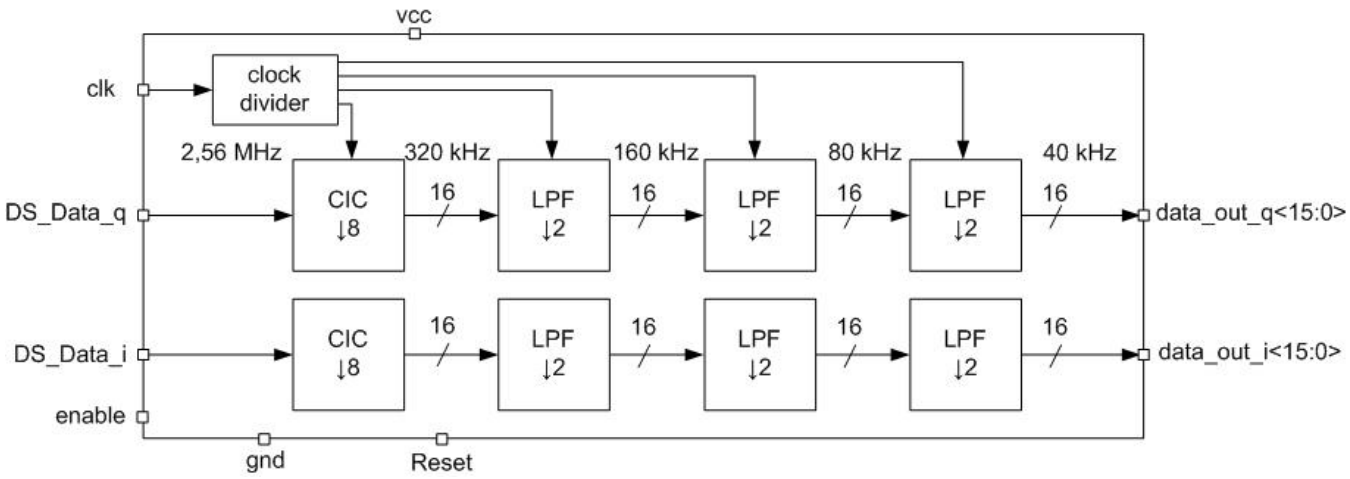

Figure 5: Digital filter structure.

5 PIN DESCRIPTION

Name	Direction	Description
DS_Data_i	I	Input single-bit complex signal
DS_Data_q	I	
clk	I	External synchronization signal
Reset	I	Reset mode
enable	I	Enable/disable
data_out_q<15:0>	O	Output 16-bit complex signal
data_out_i<15:0>	O	
vcc	IO	Supply voltage
gnd	IO	Ground

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 2.

Table 2: Block dimensions.

Dimension	Value	Unit
Height	944	um
Width	1449	um

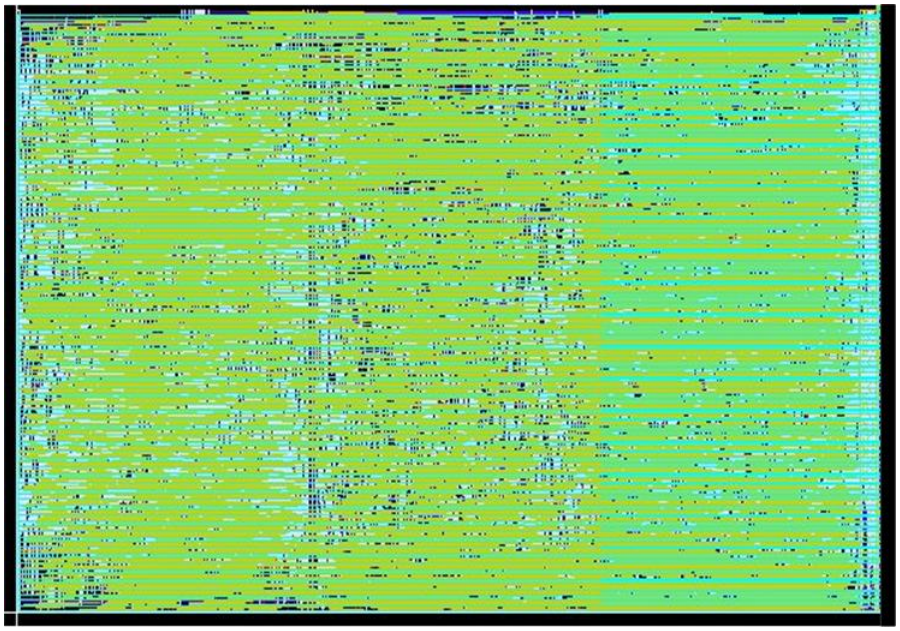

Figure 6: Digital filter layout view.

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ iHP SiGe BiCMOS 0.25 um
Status _____ silicon proven
Area _____ 1.4 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.5 ÷ 2.7 V and T_a = -45 ÷ +85 °C. Typical values are at V_{cc} = 1.8 V, T_a = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	1.5	1.8	2.7	V
Operating temperature range	T_a	-	-45	27	85	°C
Current consumption	I_{cc}	-	-	80	-	uA
Input resolution	N_{in}	-	-	1	-	bit
Output resolution	N_{out}	-	-	16	-	bit
Decimation coefficient	R	-	-	64	-	-
Input sampling rate	F_S	-	-	2.56	-	MHz
Output sampling rate	F_{Sout}	-	-	40	-	kHz
Cut-off frequency	F_{cut}	-	-	7.5	-	kHz
Rejection	A_{stop}	Frequency >20 kHz		<-60	-	dB
Input logic-high level	V_{IH}	-	$0.7V_{cc}$	-	V_{cc}+0.25	V
Input logic-low level	V_{IL}		-0.25	-	0.3	V

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optinal)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optinal)
- Documentation

REVISION HISTORY

From version 1.0:

- Section 3