704-bit EEPROM

SPECIFICATION

1 FEATURES

- SMIC EEPROM CMOS 0.18 um
- High density of memory cells
- Writing and erasing data by one high-voltage pulse
- Programming and erase time – 2 ms
- Page writes allowed
- Data retention over 10 years (endurance 10^5 cycles)
- Low power dissipation in standby and active mode
- Internally organized 44x16 bit
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

2 APPLICATION

- Access control systems
- Radio-frequency identification systems, smart cards
- Electronic devices with battery power
- Electronic tags UHF band

3 OVERVIEW

The block is a nonvolatile electrically erasable programmable read-only memory (EEPROM) with volume 704 bits (44x16), which is organized as 11 pages of 4 words by 16 bit with single-bit output data and parallel write data.
Write EEPROM page data comes to input data_in and write by words to latch through the signal sample_data, while the signal write in a state of «1». The address of a word written down in latches is defined by two low bits of the bus word_addr.
Set of flags that define the words that will be erased/written to the page is produced by signals set_flag *(3:0)*. Rst_data signal used to reset to «0» the contents of all latches before recording data, signal rst_flag – to reset to «0» all the flags erase/write before setting the required flags.
Erasing of words from page, that correspond to the flags, performed by setting a signal busy, with the signal erase is at state «1». The address of erased page is defined by four high bits of the bus word_addr. Value of the bus word_addr doesn't change throughout all cycle of deleting (while busy = «1»).
Data writing from latches to the words of page corresponding to flags, is produced by signal setting busy, thus the signal write is in a state «1». The address of writeable page is defined by four high bits of the bus word_addr.
Memory is optimized for usage in the industrial and commercial applications, requiring low power consumption and supply voltage.
The device is implemented on technology EEPROM CMOS SMIC 0.18 um.

4 STRUCTURE

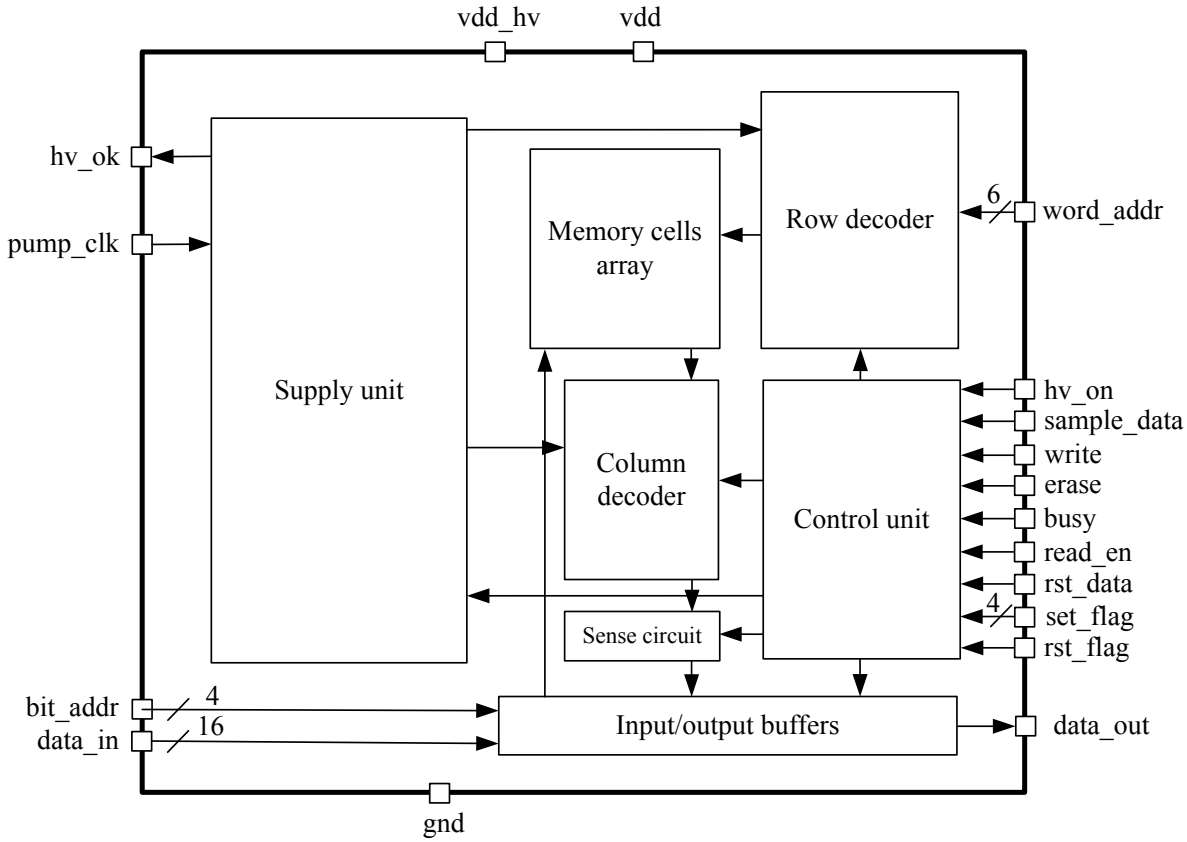

Figure 1: 704-bit EEPROM structure.

5 PIN DESCRIPTION

Name	Direction	Description
word_addr<5:0>	I	Word address
bit_addr<3:0>	I	Bit address in a word (only for read)
data_in<15:0>	I	Input data for read
sample_data	I	Control signal for input and output data
read_en	I	Read enable
rst_data	I	Common reset for input data
set_flag<3:0>	I	Set flags for erase/write cells in a separate page
rst_flag	I	Common reset erase/write flags
write	I	Write mode
erase	I	Erase mode
busy	I	Erase/write operation signal
dis_hvslope	I	Control input for smoothing of a programming voltage front
hv_on	I	Starting generation of a high voltage
pump_clk	I	Clock input for generation of a high voltage
data_out	O	Read data output
hv_ok	O	Output of a signal of readiness of a high voltage.
vdd	I/O	Supply voltage 1.8 V
vdd_hv	I/O	Unstabilized high level supply voltage (from vdd to 5 V)
gndd	I/O	Ground bus

6 LAYOUT DESCRIPTION

EEPROM layout dimensions are given in the table 1.

Table 1: Block dimensions of the EEPROM.

Dimension	Value	Unit
Height	328	µm
Width	400	µm

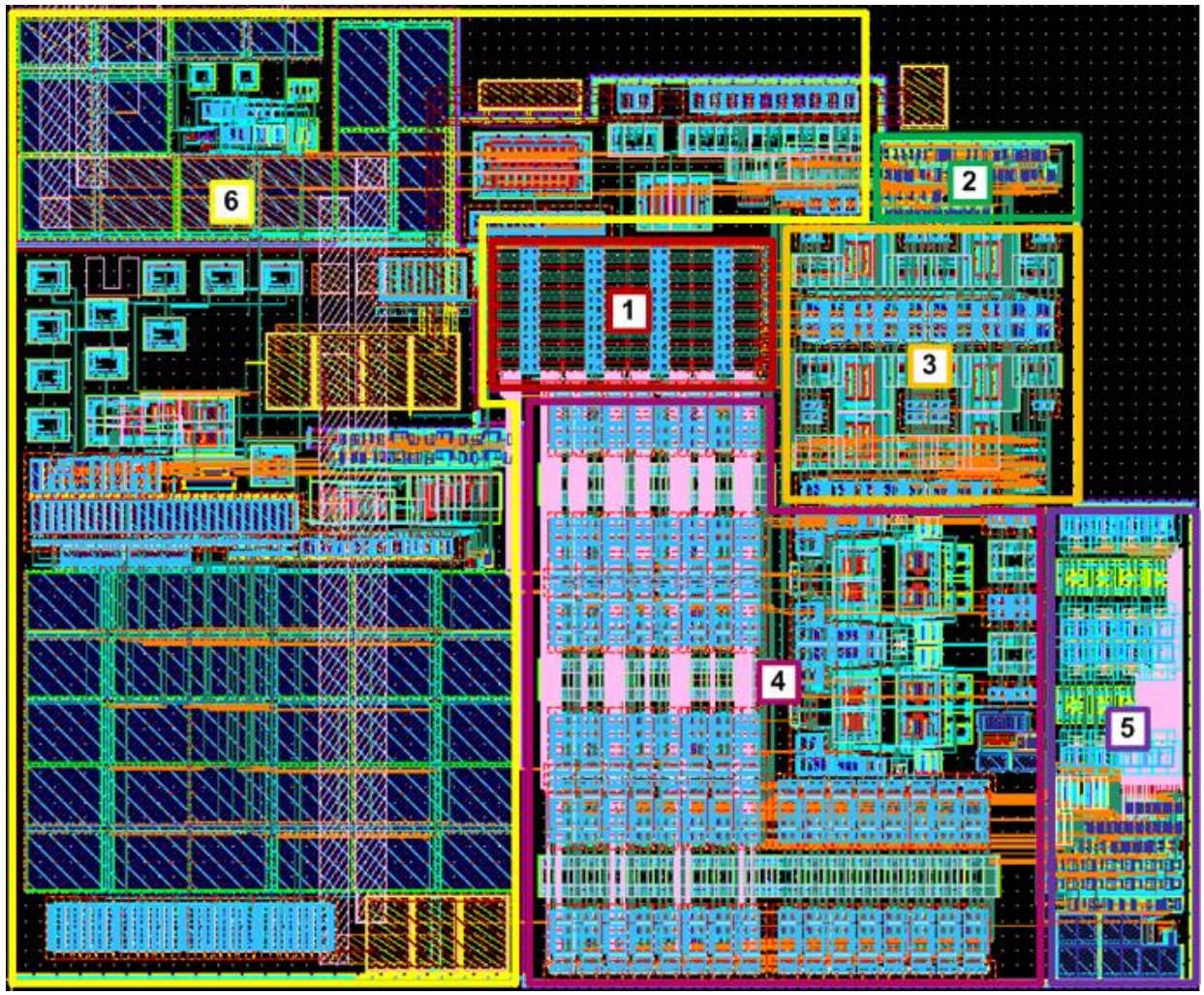

Figure 2: EEPROM layout view.

1. Memory cells array
2. Control circuit
3. Row decoder
4. Column decoder and multiplexer
5. Read/write control circuit
6. Supply module

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology SMIC EEPROM CMOS 0.18 um
Status silicon proven
Area 0.13 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd} = 1.44 ÷ 2.16 V and T = -40 ÷ +125°C. Typical values are at V_{dd} = 1.8 V and T = +27°C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Low level supply voltage	V_{dd}	-	1.44	1.8	2.16	V
High level supply voltage	V_{ddh}	-	V_{dd}	V_{dd}+0.3	5	V
Operating temperature range	T	-	-40	+27	+125	°C
Clock frequency for power supply generators	F_{clkgen}	-	-	500	-	kHz
Access time	t_{acc}	-	-	-	620	ns
Time between write and erase modes	t_{we}	-	0	-	-	us
Set/reset pulse width	t_{rs}	-	160	-	-	ns
Active pulse width of busy signal	t_{busy}	-	2000	-	2210	us
Erase setup time relative to control signal busy	t_{ers}	-	2450	-	-	us
Erase hold time relative to control signal busy	t_{erh}	-	23.8	-	23.6	us
Read setup time relative to enable signal	t_{reads}	-	2.9	-	-	us
Address setup time relative to enable signal	t_{bits}	-	0	-	-	ns
Current consumption in read mode	I_{read}	640kbit/s, V_{dd}=1.8 V	-	3.0	-	uA
Current consumption in write mode	I_{write}		-	6	-	uA
Standby current	I_{stand}	-	-	0	-	uA
High Level Input Voltage	V_{IH}	For digital inputs	0.7	-	-	V
Low Level Input Voltage	V_{IL}		-	-	0.3	V

8 DELIVERABLES

IP contents:

- Layout or blackbox
- VHDL behavioral descripton
- Documentation