512-bit EEPROM

SPECIFICATION

1 FEATURES

- SMIC EEPROM CMOS 0.18 um
- High density of memory cells
- Writing and erasing data by one high-voltage pulse
- Programming and erase time – 2 ms
- Page writes allowed
- Data retention over 10 years (endurance 10^5 cycles)
- Low power dissipation in standby and active mode
- Internally organized 16(bit per word) x 2(word per page) x 16(page) bit
- Portable to other technologies (upon request)

2 APPLICATION

- Access control systems
- Radio-frequency identification systems, smart cards
- Electronic devices with battery power
- Chip serial ID and chip safety
- Electronic tags UHF band

3 OVERVIEW

The block is a nonvolatile electrically erasable programmable read-only memory (EEPROM) with volume 512 bits (16(bit per word) x 2(word per page) x 16(page)), which is organized as 16 pages of 2 words by 16 bit with single-bit output data and parallel write data.
Write EEPROM page data comes to input **D0<15:0>** and write by words to latch through the signal **SAMPLE**, while the signal write in a state of «1». The address of a word written down in latches is defined by two low bits of the bus **adr_bl<1:0>**.
Set of flags that define the words that will be erased/written to the page is produced by signals **set_flag <*1:0*>.** Erasing of words from page, that correspond to the flags, performed by setting a signal **BUSY**, with the signal **ERASE** is at state «1». The address of erased page is defined by four high bits of the bus **adr_s<15:0>**. Value of the bus **adr_s<15:0>** doesn't change throughout all cycle of deleting (while **BUSY** = «1»).
Data writing from latches to the words of page corresponding to flags, is produced by signal setting **BUSY**, thus the signal **WRITE** is in a state «1». The address of writeable page is defined by four high bits of the bus **adr_s<15:0>**.
Memory is optimized for usage in the industrial and commercial applications, requiring low power consumption and supply voltage.
The device is implemented on technology EEPROM CMOS SMIC 0.18 um.

4 STRUCTURE

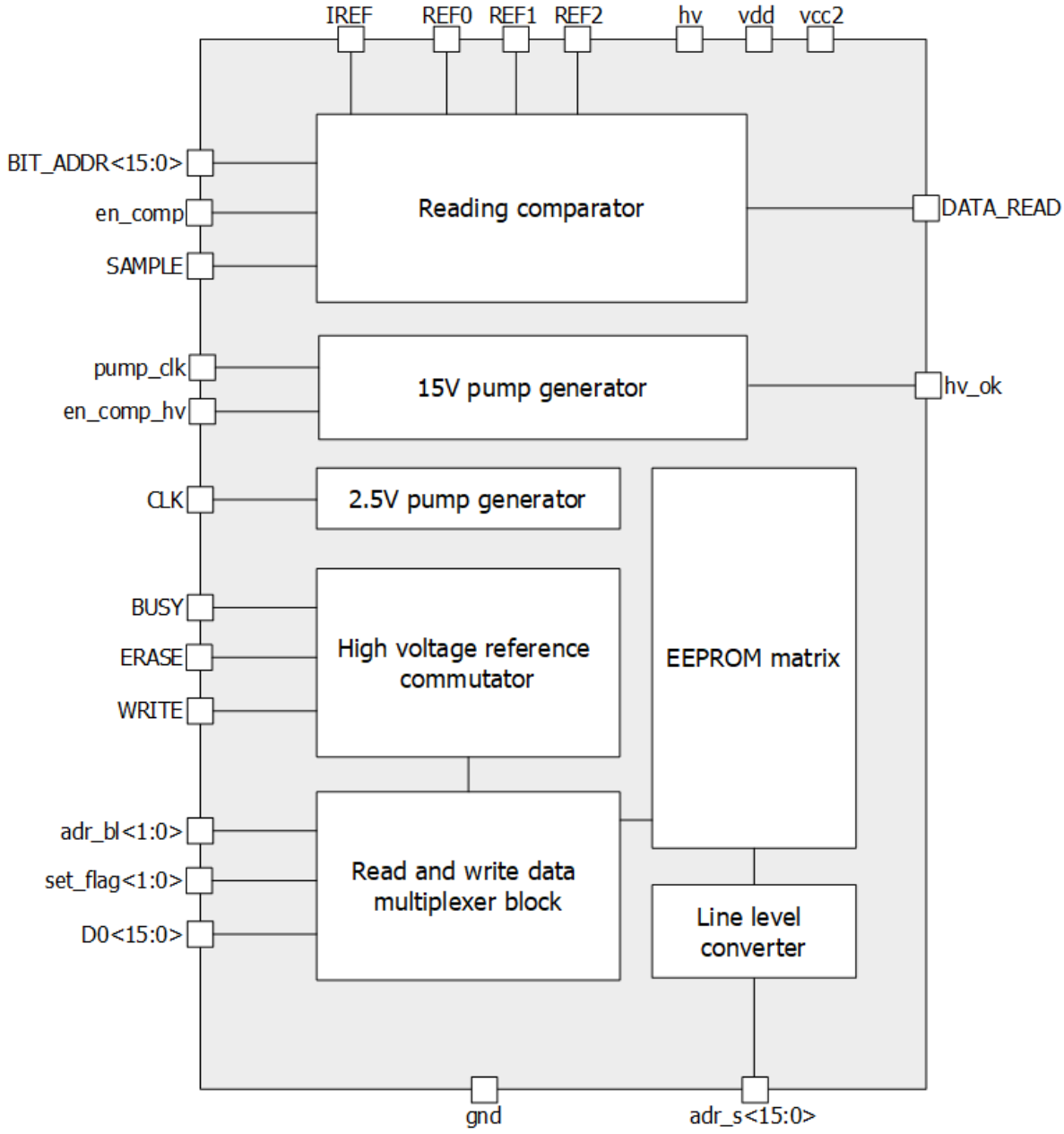

Figure 1: 512-bit EEPROM structure

5 PIN DESCRIPTION

Table 1 – EEPROM block interface signal description.

Port name	Direction for digital core	Resolution, bits	Description
REF0,REF1, REF2	input	1	Read comparator current
CLK	input	1	500kHz clock signal
pump_clk	input	1	Clock signal for high voltage pump generator
BIT_ADDR	input	16	Bit address in a word for read
adr_bl	input	2	Address of active word in a string
set_flag	input	2	Word address (within a page) to be erases/written.
adr_s	input	16	Active page address in thermometric code
EN_COMP	input	1	Enable of reading comparator
SAMPLE	input	1	Reading comparator strobe
DATA_READ	output	1	Reading comparator data
BUSY	input	1	Enable of high voltage pump generator
ERASE	input	1	Erasing signal
WRITE	input	1	Writing signal
D0	input	16	Data for writing
en_comp_hv	input	1	Enable of comparator in pump generator
hv_ok	output	1	Indicates that pump voltage is ready
IREF	input	1	Reference current (incoming)
vdd	input/output	1	Power signal
gnd	input/output	1	Ground signal
vcc2	output	1	Power signal
hv	output	1	Power supply voltage in programming mode

6 PROCEDURE WRITING / ERASING OF EEPROM CELLS

Data for writing to the EEPROM page is fed to the input ***D0*** and is written word by word, while the ***WRITE*** signal is in the logical "1" state. The address of the word in the page is determined by the the ***adr_bl*** bus (if ***adr_bl*** (1:0) = "01", the word 0 is written, if "10" – the word 1.)

The flags that define the words that will be further erased/written to the storage page are set using the ***set_flag (1:0)*** signals; in this case, ***set_flag (0)*** corresponds to the word 0, ***set_flag (1)*** corresponds to the word 1. While ***set_flag (1:0)="00***" writing will not be done. While setting While setting the ***set_flag (1:0)*** ="11", identical values from input D0 will be written in both words of the page, however, such a solution requires an increase in programming time.
For erasing or programming, the frequency **clk** and **pump_clk** as well as the set control signals and the **BUSY** signal are required. While **BUSY** = "1", switching of any control signals is not allowed.

Data is written in 2 stages: 1) erasing, 2) writing.
If writing of data is not needed, it is permissible to shorten the erasing/writing cycle by the writing phase (Tbusy for write = "0"), however, other switching and time intervals must be present. This mode can be used to increase the erasing rate or to save energy.

Erasing the words of the page that corresponds to the flags is performed by setting ***BUSY*** signal, while ***ERASE*** signal is in the logical "1" state. The address of the erasable page is determined by ***adr_s*** bus bits **(**thermometric code). The value on the ***adr_s*** bus doesn't change during the full erase and write cycle (while ***BUSY*** = "1").

The address of the written word in the page is determined by the ***adr_bl*** bus bits. The value on the ***adr_bl*** bus doesn't change during the full erase and write cycle (while ***BUSY*** = "1").
The data writing to the words of the page that corresponds to the flags is performed by setting ***BUSY*** signal, while ***WRITE*** signal is in the logical "1" state. The data recording process is shown in the figure 2.

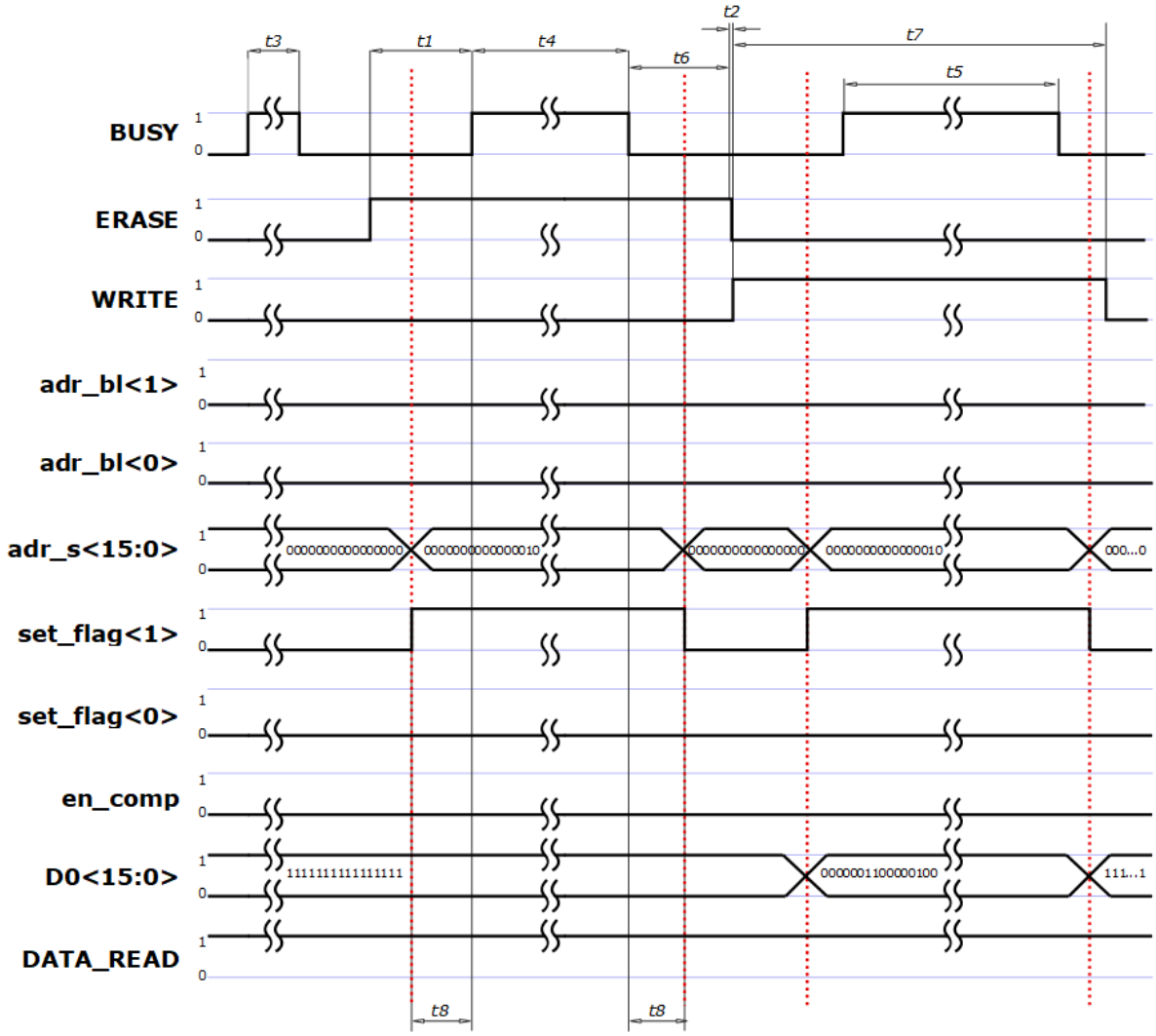

Figure 2 - Time characteristics of the EEPROM erasing/writing

The time characteristics for data erasing/writing to the EEPROM are shown in table 2.

Table 2 – Time characteristics of the EEPROM erasing/writing

Parameter	Min	Max	Units
t1	100	-	us
t2	0	-	us
t3	1216	-	us
t4	2000	2433	us
t5	2000	2433	us
t6	100	-	us
t7	2200	2633	us
t8	5	-	us

7 EEPROM READING

While EEPROM reading the ***ERASE*** and ***WRITE*** signals are in the "0" state. The ***en_comp*** signal is set to "1" which enables reading scheme. The ***adr_s*** bus is supplied with page address; the ***BIT_ADDR*** bus is supplied with the bit address in the word. Then the ***SAMPLE*** signal is set to "1" enables a reading comparator. After switching the signal sample to "0", the last read value is stored in latch. After the ***SAMPLE*** or ***BIT_ADDR*** signals changing, the ***DATA_READ*** output provides the value of the selected bit.
After changing **adr_bl** or **adr_s**, it is necessary to pause > 10 µs before reading the next data bit. Switching to **BIT_ADDR** does not require a pause. The reading procedure is shown in the figure 4. The time characteristics of the EEPROM reading is shown in table 3.

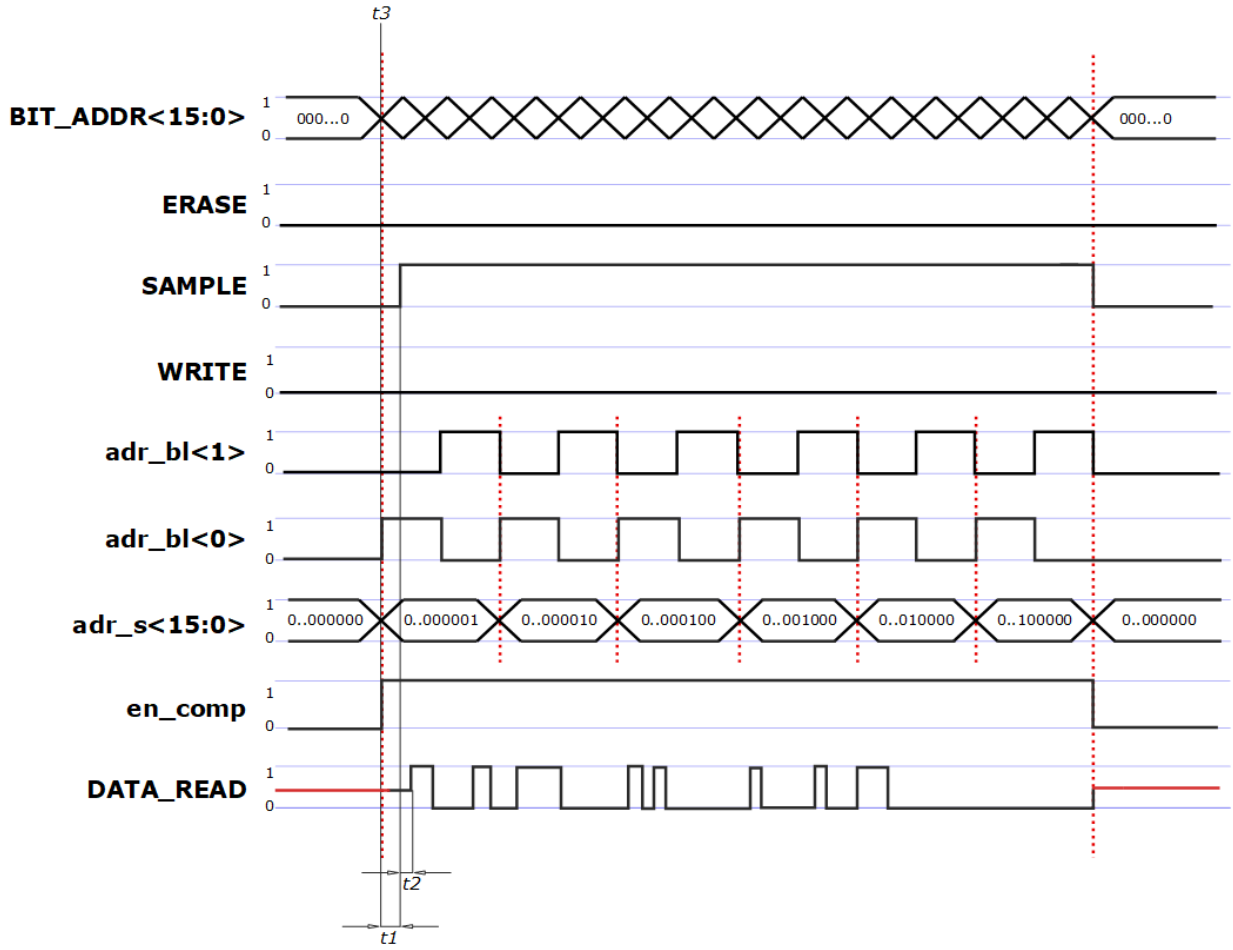

Figure 3 - Time characteristics of the EEPROM reading

Table 3 – Time characteristics of the EEPROM reading

Parameter	Min	Max	Units
t1	0.891	-	us
t2	200	620	ns
t3	0	-	ns

8 LAYOUT DESCRIPTION

EEPROM layout dimensions are given in the table 4.

Table 4 – Block dimensions of the EEPROM.

Dimension	Value	Unit
Height	328	µm
Width	169	µm

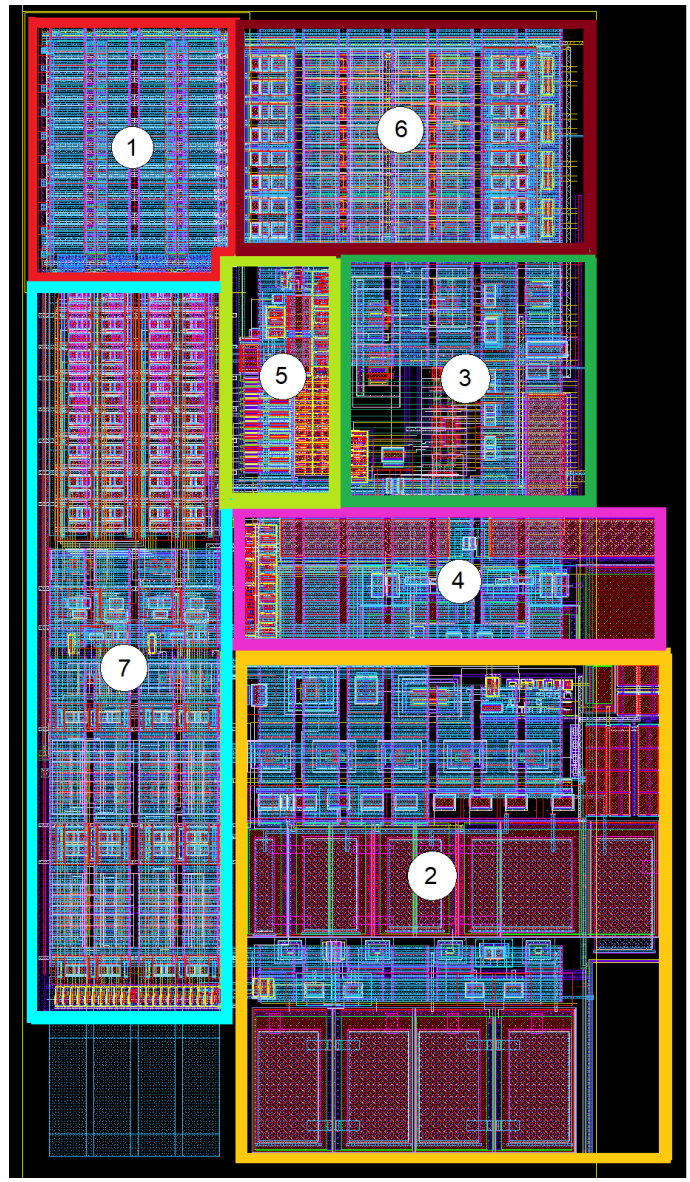

Figure 4 - EEPROM layout view

1. EEPROM matrix
2. 15V pump generator
3. High reference voltage commutator
4. 2.5V pump generator
5. Reading comparator
6. Line level converter
7. Read and write data multiplexer block

9 OPERATING CHARACTERISTICS

9.1 TECHNICAL CHARACTERISTICS

Technology SMIC EEPROM CMOS 0.18um
Status silicon proven
Area $0.055mm^2$

9.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for $V_{dd} = 0.7 \div 1.8$ V and T = -40 ÷ +125°C. Typical values are at $V_{dd} = 1$ V and T = +27°C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Low level supply voltage	V_{dd}	-	0.7*	1	1.8	V
Operating temperature range	T	-	-40	+27	+125	°C
Clock frequency for power supply generators	F_{clkgen}	-	-	500	-	kHz
Access time	t_{acc}	-	-	-	620	ns
Time between write and erase modes	t_{we}	-	0	-	-	us
Set/reset pulse width	t_{rs}	-	160	-	-	ns
Active pulse width of busy signal	t_{busy}	-	2000	-	2210	us
Erase setup time relative to control signal busy	t_{ers}	-	2450	-	-	us
Erase hold time relative to control signal busy	t_{erh}	-	23.8	-	23.6	us
Read setup time relative to enable signal	t_{reads}	-	2.9	-	-	us
Address setup time relative to enable signal	t_{bits}	-	0	-	-	ns
Current consumption in read mode	I_{read}	Fclk = 512KHz	198	314	802	nA
Current consumption in write mode	I_{write}	Fclk = 512KHz, Fpump=1MHz	1.178	2.2	9.51	uA
Standby current	I_{stand}	-	-	0	-	uA
High Level Input Voltage	V_{IH}	For digital inputs	0.7	-	-	V
Low Level Input Voltage	V_{IL}		-	-	0.3	V

***Note** – When Vdd drops below 1 V to 0.7 V (wherein, Fclk = 512kHz, Fvcc2 = 512kHz, F_pump = 1MHz): In this case, writing occurs, but hv_ok does not. Verification of the writing should be done by reading after writing.

10 DELIVERABLES

IP contents:

- Schematic in electronic format (.netlist file)
- Layout in GDSII electronic format (.gds file)
- Abstract view in electronic format (.lef and .lib files)
- DRC, LVS, antenna reports in electronic format (.summary, .report files)
- Datasheet in electronic format (.pdf file)