USB 2.0 High/Full-Speed interface

SPECIFICATION

1 FEATURES

- SMIC CMOS 180 nm
- USB 2.0 specification compliant
- Multiple data rates support: Full Speed (12 Mbit/sec), High Speed (480 Mbit/sec)
- 4 data endpoints (Bulk/Interrupt type): 2 IN, 2 OUT
- 512 byte memory buffers for each endpoint for data transfer between endpoint and microcontroller
- INOUT control endpoint used for interface initialization and control procedures according to USB 2.0 specification
- Two 64 byte memory buffers for control endpoint
- Direct Memory Access to data endpoints
- IN or OUT endpoint dual-buffered mode (Ping-Pong)
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATIONS

- Integrated microcontroller systems
- Communication and data transfer systems

3 FUNCTIONAL DESCRIPTION

IP acts as USB controller compliant to USB2.0 specification and can operate at USB Full Speed (12 Mbit/sec) and High Speed (480 Mbit/sec) rates. Interface supports 4 Bulk/Interrupt data endpoints – 2 IN (address 1 and 3, microcontroller-to-host) and 2 OUT (address 2 and 4, host-to-microcontroller). Each endpoint has 512 byte memory buffer to transfer data between endpoint and microcontroller. Also interface has control endpoint (address 0, bidirectional) used for interface initialization and control according to USB 2.0 specification. Control endpoint has two 64 byte memory buffers (for each direction). Ping-pong mode can be used to speed up data transfer for IN or OUT endpoint. In this mode one endpoint buffer is available for USB data bus while other endpoint buffer can be accessed by microcontroller; access to buffers is performed through one pipe in this mode (logically only one endpoint is used). Interface communicates with microcontroller via APB bus.
The device is implemented on technology SMIC CMOS 180 nm.

4 STRUCTURE

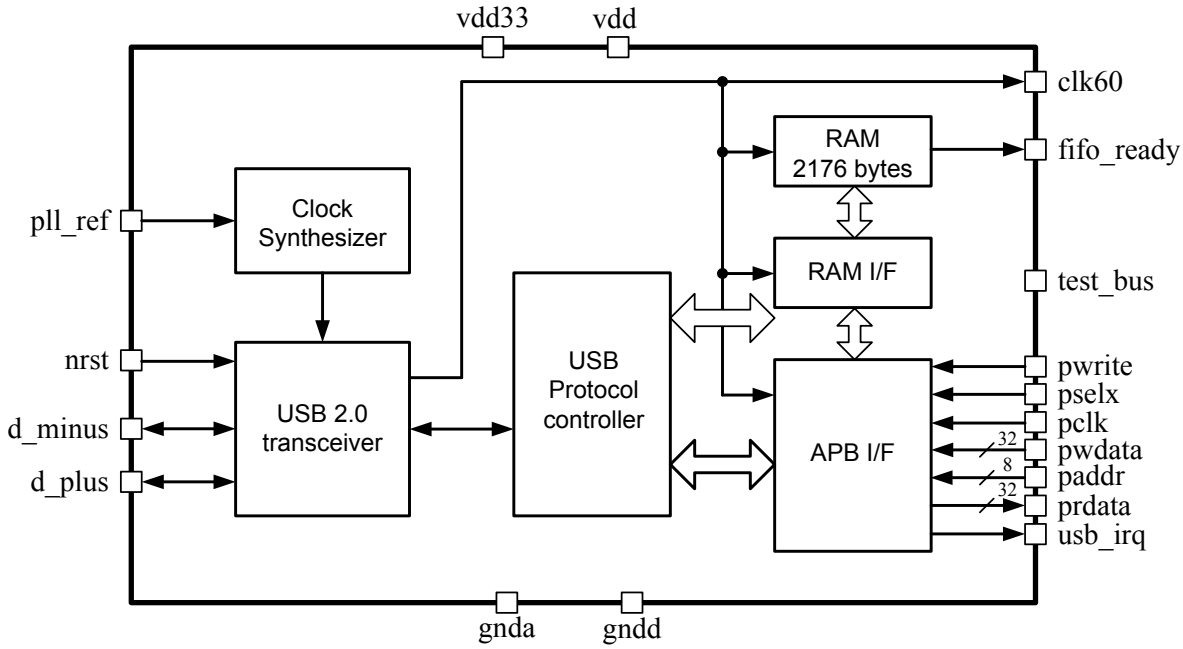

Figure 1: USB 2.0 High/Full-Speed interface structure.

5 PIN DESCRIPTION

Name	Direction	Description
pll_ref	I	PLL reference clock
nrst	I	Reset
pwrite	I	APB write enable
pselx	I	APB select
pclk	I	APB bus clock
pwdata<31:0>	I	APB data input
paddr<7:0>	I	APB address input
prdata<31:0>	O	APB data output
usb_irq	O	Interrupt request
fifo_ready	O	FIFO buffer ready
test_bus<13:0>	O	Test bus
clk60	O	Output clock 60 MHz
d_minus	I/O	USB differential bus
d_plus		
vdd33	I/O	Analog power supply 3.3V
vdd	I/O	Digital power supply 1.8V
gnda	I/O	Analog ground
gndd	I/O	Digital ground

6 LAYOUT DESCRIPTION

Table 1: IC dimensions.

Dimension	Value	Units
Height	896	µm
Width	625	µm

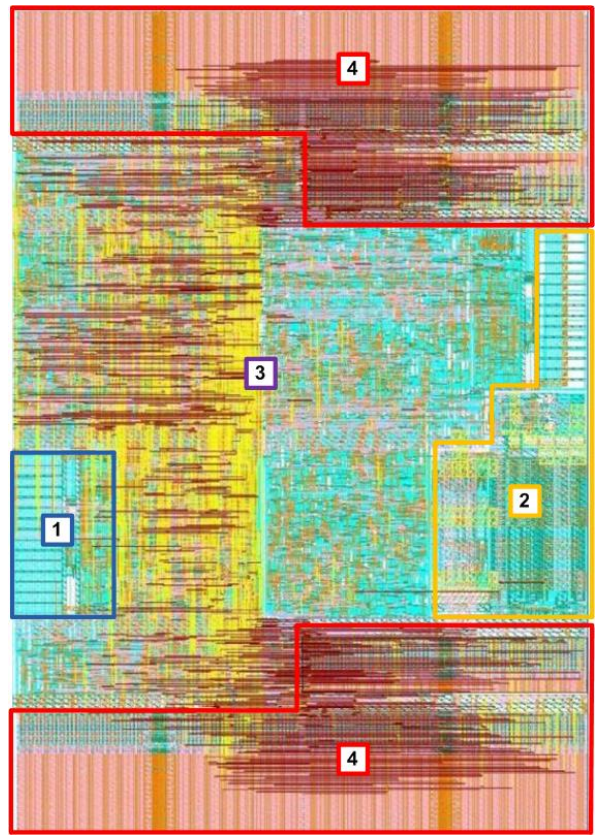

Figure 2: USB interface topology overview

1. PLL block
2. Transceiver
3. Logic block
4. RAM blocks

7 OPERATION CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology SMIC CMOS 180 nm
Status silicon proven
Area $0.56mm^2$

7.2 ELECTRICAL CHARACTERISTICS

Electrical characteristics apply for following conditions: V_{dd33} = 2.97 ÷ 3.63V, V_{dd}= 1.62 ÷ 1.98V and T = -40 ÷ +125 °C. Typical values: V_{dd33}= 3.3V, V_{dd}= 1.8V, T = + 27 °C, if not other specified

Parameter	Symbol	Cond.	Value			Units
			min	typ	max	
Analog part supply voltage	V_{dd33}	-	2.97	3.3	3.63	V
Digital part supply voltage	V_{dd}	-	1.62	1.8	1.98	V
Operation temperature range	T	-	-40	+27	+125	°C
Current consumption	I_{cn}	High speed	-	-	20	mA
Standby current	I_{st}	-	-	-	12	µA
Input clock frequency	F_{clk}	-	-	8	-	MHz
Data rate	F_{HIGH}	-	-	480	-	Mbit/sec
	F_{FULL}	-	-	12	-	Mbit/sec

8 DELIVERABLES

IP contents:

- Layout View (GDSII)
- Evaluation kit based on packaged IC
- Characterization Report
- Behavioral Model
- SPICE netlist (.cdl)
- Integration Support
- Documentation